Crystal Image through
Imaging Innovation

PIXELPLUS

Brief Datasheet

1/4" HD Bayer CMOS Image Sensor with 1280x720 Pixel Array

PS7100K

Rev 0.0

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▶ Features

▷ 1296 x 736 Effective pixel array with RGB bayer color filters and micro-lens

▷ Support Output format
- 10 bit RGB bayer

▷ Interface
- 10 bit Digital parallel

▷ Auto black level compensation

▷ White balance gain

▷ Programmable frame size, frame rate, Window size, image orientation and exposure

▷ Horizontal / Vertical mirroring and cropping

▷ External synchronization support (Genlock)

▷ Chip address selection PAD

▷ Software Reset

▷ On-chip Phase Locked Loop (PLL)

▷ I2C Interface support

▷ 40 CSP Package type supports

Pixel Size	2.80 um x 2.80 um
Effective Pixel Array	1296 (H) x 736 (V)
Effective Image Area	3.689 mm x 2.061 mm
Optical Format	1/4 inch
Input Clock frequency	4 ~ 27Mhz
Max. Frame Rate	60 fps
Dark Signal	TBD [mV/sec] @ 60℃
Sensitivity	TBD [V/Lux.sec]
Power Supply	HVDD : 1.8 ~ 3.3V AVDD : 3.3V PLVDD : 3.3V
Power Consumption	TBD mW @ Dynamic
	TBD uW @ Standby
Operating Temp. (Fully Functional Temp)	-40 ~ 105 [℃]
Dynamic Range	TBD [dB]
SNR	TBD [dB]

[Table 1] Typical Parameters

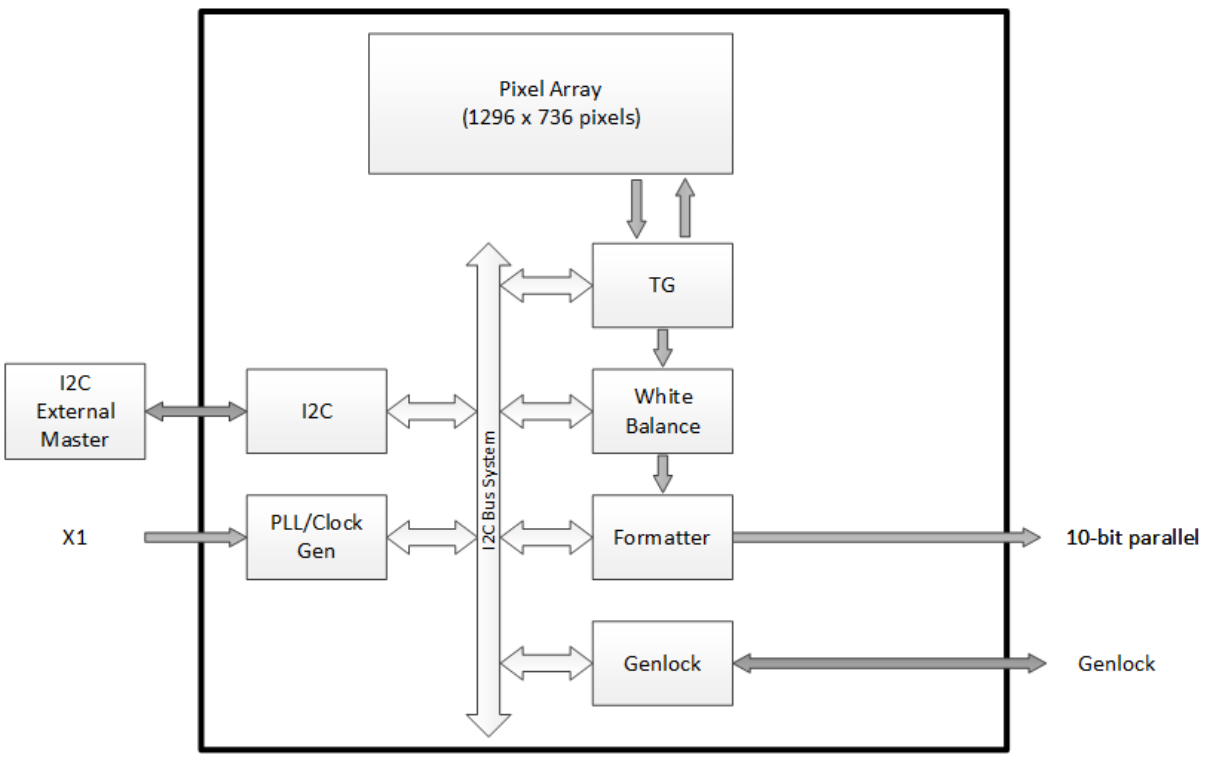
▶ Signal Environment

Due to having intolerable input pads, the input signal must have HVDD power level for stable operation. If the power of input signal is higher that the recommended level, leakage current may flow via short circuit path in the input pads.

▶ Chip Architecture

PS7100K has 1296 x 736 effective pixel array and includes column/row driver circuits for reading out pixel data progressively. CDS circuit reduces noise generated from various sources, which mainly are resulted from process variations. Pixel output level is compared with the reset level of the pixel, and the difference between the two levels is sampled, thus reducing fixed error signal level. Each of R, G, B pixel output can be multiplied by different gain factors to balance the color of images in various light conditions. The analog signals are converted into digital data one line at a time and each line data is streamed out column by column. The Bayer RGB data is passed through a sequence of image signal processing to produce bayer output data. PS7100K supports several output interfaces such as 10-bit parallel.

Control of internal functions or output signal timings is achieved by modifying registers directly through 2-wire serial interface called I2C.



[Fig. 1] Block Diagram

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