Crystal Image through
Imaging Innovation

PIXELPLUS

Brief Datasheet

# 1/3" NTSC/PAL CMOS Image Sensor with 960x576 Pixel Array

# PC1058K

**Rev 0.0**

**Last Update : 21. Jun. 2017**

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## ▶ Features

▷ 976 x 592 Effective pixel array with
RGB bayer color filters and micro-lens

▷ Power supply :
HVDD/CVDD/AVDD=3.3V

▷ Input. Clock Frequency : 27MHz

▷ Output formats
◆ Composite Output mode
- CVBS ( NTSC/PAL )

◆ Digital Output mode
- max. 960x576 @ YUV422/RGB565/RGB444
- max. 960x576 @ Bayer

◆ Analog/Digital Output mode
- ITU-R. BT1302 (960x240/288)

▷ Image processing on chip
lens shading, gamma/defect/color correction
NR (2D noise reduction), color interpolation,
edge enhancement, brightness, contrast
auto black level, auto white balance
auto exposure control
and back light compensation

▷ Free scaling (Up&Down)

▷ Smart Contrast : Adaptive D-WDR & Contrast

▷ Selective Color Shift

▷ PlusPixel4.0TM Technology Applied

▷ High Image Quality
And Ultra low light performance

▷ I2C & SPI master include

▷ 4 layer overlay functions by using SPIROM

▷ On chip Phase Locked Loop (PLL)

▷ Cropping & max 4X Digital Zoom support

| | |
|---|---|
| **Pixel Size** | 5.00 um x 6.20 um |
| **Effective Pixel Array** | 976 (H) x 592 (V) |
| **Effective Image Area** | 4.88 mm x 3.67 mm |
| **Optical Format** | 1/3 inch |
| **Input Clock frequency** | 27Mhz |
| **Frame Rate** | 60 field / sec @ NTSC<br>50 field / sec @ PAL |
| **Dark Signal** | 47.6 [mV/sec ] @ 60℃ |
| **Sensitivity** | 10.9 [V/Lux.sec] |
| **Power Supply** | Analog : 3.3V<br>HVDD : 3.3V<br>CVDD : 3.3V |
| **Power Consumption** | 486.2 mW @ NTSC<br>452.1 mW @ PAL |
| | 466.4 uW @ Standby |
| **Dynamic Range** | 61.8 [dB] |
| **SNR** | 43.3 [dB] |

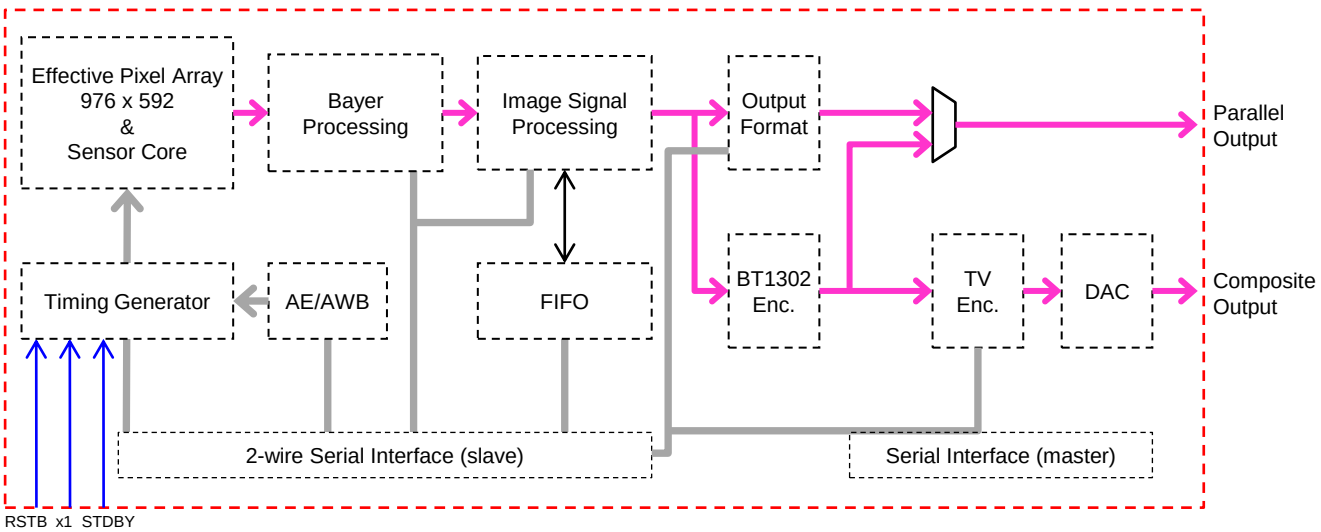
[Table 1] Typical Parameters

## ▶ Signal Environment

PC1058K don't have tolerant Input pads. The input signal must be equal to HVDD for stable operation. If the power of input signal is higher than recommended, it may flow leakage current by shot circuit path in the input PADs.

## ▶ Chip Architecture

PC1058K has 976 x 592 effective pixel array and column/row driver circuits to read out the pixel data progressively. CDS circuit reduces noise signals generated from various sources mainly resulting from process variations. Pixel output is compared with the reset level of its own and only the difference signal is sampled, thus reducing fixed error signal level. Each of R, G, B pixel output can be multiplied by different gain factors to balance the color of images in various light conditions. The analog signals are converted to digital forms one line at a time and 1 line data are streamed out column by column. The Bayer RGB data are passed through a sequence of image signal processing blocks to finally produce YCbCr 4:2:2 output data. Image signal processing includes such operations as gamma correction, defect correction, low pass filter, color interpolation, edge enhancement, color correction, contrast stretch, color saturation, white balance, exposure control and back light compensation. Internal functions and output signal timing can be programmed simply by modifying the register files through 2-wire serial interface.




[Fig. 1] Block Diagram

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